The following Listing of Claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

1. (Currently Amended) A method for fabricating a test pattern wafer suitable for CMP characterization, comprising:

providing a silicon substrate;

depositing a layer of oxide over a first surface of the silicon substrate;

defining a test pattern structure over a surface of the layer of oxide, the defining including selecting from a plurality of test pattern geometries, densities and complexities of features, and using an appropriate test pattern mask to arrange the selected features in a test pattern;

fabricating the test pattern structure over the layer of oxide;

characterizing a CMP process using the test pattern wafer; and

removing the test pattern structure and the oxide layer from the silicon substrate.

2. (Canceled)

3. (Original) A method for fabricating a test pattern wafer suitable for CMP characterization as recited in claim 1, wherein the fabricating the test pattern structure includes making simulated transistor features in and over the layer of oxide, and depositing a layer of high density plasma fill over the simulated transistor features.

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4. (Original) A method for fabricating a test pattern wafer suitable for CMP characterization as recited in claim 3, wherein the characterizing of the CMP process includes measuring a rate of removal of the high density plasma fill, measuring a thickness of simulated transistor features, and evaluating a degree of precision of the CMP process.

5. (Original) A method for fabricating a test pattern wafer suitable for CMP characterization as recited in claim 1, wherein the removing of the test pattern structure and the oxide layer from the silicon substrate allows the wafer to be reclaimed and used for subsequent test pattern wafer fabrication.

6. (Currently Amended) A method for reclaiming a silicon substrate for repeated chemical mechanical polishing (CMP) characterization, comprising:

forming a sacrificial oxide layer over the silicon substrate;

forming test features in the sacrificial oxide layer;

etching shallow trench isolation (STI) trenches in the sacrificial oxide layer;

depositing high density plasma in the STI trenches and over the test features;

performing CMP characterization using the test features, the test features providing data regarding CMP performance; and

stripping the sacrificial oxide layer including the test features, the stripping enabling reuse of the silicon substrate for the repeated CMP characterization.

7. (Canceled)

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8. (Currently Amended) A method for reclaiming a silicon substrate for repeated chemical mechanical polishing (CMP) characterization as recited in claim ~~7~~ 6, wherein the performing of the CMP characterization includes removing the high density plasma from over the test features using a CMP process, and measuring performance indicators of the CMP process during the removing.

9. (Original) A method for reclaiming a silicon substrate for repeated chemical mechanical polishing (CMP) characterization as recited in claim 8, wherein the performance indicators include a rate of removal of the high density plasma, a thickness of the test features after the CMP process, and a surface planarity of a resulting surface over the test features.

10. (Currently Amended) A method for reclaiming a substrate for repeated chemical mechanical polishing (CMP) characterization, comprising:

forming a sacrificial oxide layer over the substrate, the oxide layer being configured to act as a silicon substrate;

forming test features into the sacrificial oxide layer, the test features designed to simulate transistor structures and including shallow trench isolation (STI) structures, the STI structures including STI trenches etched into the sacrificial oxide layer;

performing CMP characterization of the test features, the test features providing data regarding CMP performance over the simulated transistor structures; and

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stripping the sacrificial oxide layer including the test features, the stripping enabling reuse of the substrate for the repeated CMP characterization without damage to the substrate.

11. (Original) A method for reclaiming a substrate for repeated chemical mechanical polishing (CMP) characterization as recited in claim 10, wherein the sacrificial oxide layer is formed to a depth of about 2000Å - 5000Å, and configured to preserve a structure and an integrity of the substrate.

12. (Canceled)

13. (Currently Amended) A method for reclaiming a substrate for repeated chemical mechanical polishing (CMP) characterization as recited in claim ~~12~~ 10, further comprising depositing high density plasma into the STI trenches.

14. (Original) A method for reclaiming a substrate for repeated chemical mechanical polishing (CMP) characterization as recited in claim 13, wherein the CMP characterization of the test features includes removing an overburden of high density plasma until the high density plasma in the STI trenches forms a planar surface with a top surface of the simulated transistor structures.

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15. (Currently Amended) A method for reclaiming a substrate in chemical mechanical polishing (CMP) characterization of simulated transistor structures, comprising:

forming a sacrificial layer over the substrate, the layer being configured to structurally simulate a silicon substrate;

forming simulated transistor structures using the sacrificial layer, the using the sacrificial layer including forming shallow trench isolation (STI) trenches in the sacrificial layer to a depth of about 3000Å - 4000Å;

performing CMP characterization of the simulated transistor structures, the characterization providing data regarding CMP performance over the simulated transistor structures; and

stripping the sacrificial layer including the simulated transistor structures, the stripping enabling reclaiming of the substrate for repeated CMP characterization;

wherein the reclaiming enables forming of additional sacrificial layers, forming of additional simulated transistor structures, performing of additional CMP characterization, and additional stripping.

16. (Canceled)

17. (Currently Amended) A method for reclaiming a substrate in chemical mechanical polishing (CMP) characterization of simulated transistor structures as recited in claim ~~16~~ 15, wherein the simulated transistor structures include simulated transistor

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gate structures, the simulated transistor gate structures being formed with at least one layer of silicon nitride.

18. (Original) A method for reclaiming a substrate in chemical mechanical polishing (CMP) characterization of simulated transistor structures as recited in claim 17, wherein the simulated transistor structures are formed in a plurality of structure densities, structure complexities, and structure geometries.

19. (Original) A method for reclaiming a substrate in chemical mechanical polishing (CMP) characterization of simulated transistor structures as recited in claim 18, wherein the data regarding CMP performance includes a rate of removal, a depth of the at least one layer of silicon nitride, and a degree of planarization of a resulting surface over the simulated transistor structures.

20. (Currently Amended) A method for fabricating a test pattern wafer for repeated chemical mechanical polishing (CMP) characterization, comprising:

forming a sacrificial oxide layer over a silicon substrate, the sacrificial oxide layer being configured to act as the silicon substrate;

forming test features into the sacrificial oxide layer, the test features formed to simulate semiconductor structures;

performing CMP characterization of the test features, the test features providing data regarding CMP performance over the simulated semiconductor structures; and

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stripping the sacrificial oxide layer including the test features from the test pattern wafer, the stripping enabling reuse of the silicon substrate for subsequent fabrication of a new test pattern wafer and repeated CMP characterization without damage to the silicon substrate,

wherein the forming of the test features includes selecting from a plurality of test pattern geometries, densities and complexities of features, and using an appropriate test pattern mask to arrange selected features in a test pattern die.

21. (Original) A method for fabricating a test pattern wafer for repeated chemical mechanical polishing (CMP) characterization as recited in claim 20, wherein the test features include shallow trench isolation trenches and simulated transistor gate structures.

22. (Currently Amended) A method for fabricating a test pattern wafer for repeated chemical mechanical polishing (CMP) characterization as recited in claim 20, wherein the test features include one or a combination of tungsten plugs, copper patterns ~~dielectrics~~, and interlayer dielectrics.

23. (Canceled)

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